Progress and Testing Challenges of Large-aperture Digital Phased Array

Speaker:
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Tron Future Tech Inc.

Our Mission:
• We help our customers collect, analyze and utilize valuable data through fundamental sensor and communication inventions.

Area of Focus:
• Ultrathin all-digital/hybrid phased array based radar/communication turnkey systems.
• Value-added data processing infrastructure.

Major Capabilities:
• IC design: III/V RFFE, CMOS RFSoC, ASIC
• Module design: Power, FPGA, GPU modules
• Hardware system design: SatCom, AESA Radar
• Software system design: cloud service

About Us:
>20% employee with Ph.D. degrees from Caltech/USC/MIT/UCLA/NTU/NCTU/NTHU etc.

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Our History and Experiences

Chip Level

- 2006: 77GHz Phased-Array ICs (Participation)
- 2007: 1-15GHz Phased-Array ICs (Participation)
- 2008: 6-18GHz Phased-Array ICs (Participation)
- 2008: 79GHz Radar
- 2010: 35GHz Phased Array

Package Level

- 2008: 3D Device Stacking
- 2008: Crystal Resonator
- 2008: 3D Flexible System
- 2010: 35GHz 768-Element Hybrid AESA
- 2012: S-band Digital RF Front-End
- 2013: Phased-Array ICs (Participation)
- 2015: X-band Phased Array
- 2016: Heterogeneous Integration Platform
- 2017: Ka-Band Digital RF Front-End
- 2018: S-band Digital RF Front-End
- 2019: Wideband X-band Digital RF Front-End
- 2020: QFN Production
- 2021: High-reliability packaging

System

- 2006: 77GHz
- 2007: 1-15GHz
- 2008: 1-18GHz
- 2008: 6-18GHz
- 2010: 35GHz
- 2012: 35GHz 768-Element Hybrid AESA
- 2013: X-band Portable AESA Radar
- 2015: S/X-band Portable AESA Radar
- 2016: Data API
- 2017: Satellite Downlink
- 2018: Satellite SAR
- 2019: Satellite SAR

Total Solution
Agenda

• Technology Progress Overview.

• Market Segmentation.

• Testing Challenges.
Let's Imagine Future AESA
(and ignoring technological feasibility for 30 seconds….)

1. Paper thin, and probably flexible.
2. Include all Radar/COM/EW functions and very easy to use.

Two fundamental problems need to be addressed:

1. To what extent can this ideal concept be fundamentally possible?
2. How feasible are the underlying technologies today?

• What breakthroughs have been made in technology?
  1. **Arithmetic and Logic Circuit** → 80x size & performance improvement in last 12 years.
  2. **Analog-to-Digital Converter** → 5x size & power improvement in 10 years.
  3. **RF Power Amplifier** → GaN PA generates 10x more power with >50% efficiency.
  4. **Transceiver Modules** → discrete to integrated TR module, >100 times size reduction.
  5. **Packaging and Assembling** → 3D-IC-stacking ball grid array (BGA) with flip-chip process.

Ref: Our EW Europe 2018 Talk:” Flexibility and Thinness – How Semiconductor Technologies Shape Future Radar and Electronic Warfare?”
A Possible Future X-band Array Element

- Antenna is fundamentally limited by (signal wavelength) times (fractional bandwidth) $\sim \left( \frac{\lambda_0 \cdot \Delta f}{f_C} \right)$.
- Electronics will be limited by capacitors, inductors and filters ($\Rightarrow$ switching speed & material properties).
- Element-level functions will be 3D heterogeneously integrated/packaged. Several challenges:
  - Mechanical stress, and heat exchange.
- The package has to be mounted on a substrate (AlN or graphene on Si/SiC) with a thickness of 300-500 $\mu$m to provide mechanical strength.
The thickness is mainly limited by how heat and DC power are transferred. For 10GHz system, 3-15 mm subarray thickness and 2-15 mm global mounting structure (secondary or higher hierarchy) can be achieved. This make it possible to achieve ~3mm lower-power hundred-element array at X-band, <30mm thickness for THAAD-grade radar within a decade.
Scalable Subarray 2018 Prototype (4x4)

Subarray Architecture

- TR AiP Module
- TR AiP Module
- TR AiP Module
- LOs/Trigger Buffers
- Power Module 1
- Power Module 2
- Signal Processor
- 28V (nom.)
- 20-60V DC
- LOs/Trigger
- Power
- I/Os
- Control
- LOs/Trigger Buffers
- Serdes

Top View

- Demonstrator Debug Port
- TR Module
- Demo. mount
- 64 mm

Side View

- 35.6 mm

- TR AiP modules
- Interposer: 2.6 mm, 2.8 mm
- Power Module 1: 1.6 mm, 7.4 mm
- Signal Processor: 1.8 mm, 7.4 mm
- Power Module 2: 1.6 mm

Element-level digital AESA with cm-thickness.

2018 prototype
The LTCC Multichip TR Modules and AiP

- The RF SoC can work with several GaAs and GaN frontends (LNA/PA).
- This is 2018 RD prototype, not a product.

**Operational Frequency**
- Band: 9-10 GHz
- Channel BW: 40 MHz

**A Typical GaAs Frontend**
- PA Power: 27 dBm
- LNA Gain: 16 dB
- LNA NF: 2.5 dB
- Switch Time: 1 ns

**CMOS RF SoC**
- Transmitter
- Receiver
- Digital Input
- RF Input
- RF Output
- Digital Output
- Synchronized CLK Distribution

**Package Size**
- 15.3 mm x 15.3 mm x 3 mm
- 2.6 mm (assembled thickness)
Early 4x8 Array Pattern Measurement
- Measured peak EIRP ~ 48 dBm with 32 CMOS only TXs.

Wireless Scanning Technology Development

**AESA**
Active Electronically Scanned Array

**PESA**
Passive Electronically Scanned Array

**Mechanically Scanned Antenna**

<table>
<thead>
<tr>
<th>Mechanically Scanned Antenna</th>
<th>Electronically Scanned Array</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single RF Transceiver</td>
<td>Multiple RF Transceiver</td>
</tr>
</tbody>
</table>

**Analog Complexity** (RF Transceiver)

**Digital Complexity** (Digital Signal Process)

Ref: EW Asia 2019: "Ultrathin All-Digital Software-defined Active Phased Array Technology"
The cost of phased array is proportional to the total no. of array elements and PA power.

3D AESA Cost Reduction

- Fully Populated Planar AESA.
- Orthogonal Linear Digital AESA.

<table>
<thead>
<tr>
<th>No. of Elements</th>
<th>$W \times H$</th>
<th>$H$ (TX), $W$ (RX)</th>
<th>1024 $\Rightarrow$ 32 (3% cost)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Power</td>
<td>$P_0 \times W \times H$</td>
<td>$\sim P_0 \times (H)$</td>
<td>3% original power</td>
</tr>
<tr>
<td>Antenna Gain</td>
<td>$\propto W \times H$</td>
<td>$\propto W$ (RX), $\propto H$ (TX)</td>
<td>3% gain for RX &amp; TX</td>
</tr>
<tr>
<td>Max. Dwell Time</td>
<td>$T_0$</td>
<td>$T_0 \times H$</td>
<td>32 times with RX multibeam</td>
</tr>
<tr>
<td>SNR</td>
<td>$SNR_0$</td>
<td>$SNR_0 \cdot H / H^3$</td>
<td>$1/1024 \Rightarrow (18%$ detection range$)$</td>
</tr>
<tr>
<td>Cost per Area</td>
<td>$C_0$</td>
<td>$C_0$</td>
<td>Similar cost per coverage area.</td>
</tr>
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An Urban Surveillance Scenario
3D Detection with 16TX, 24RX

• “3D” position of an RCS target can be extracted.
  • Curvature of high-way can be precisely measured from a remote site.
• Ground surface estimation and target pattern recognition is used to identify drone from clutters(cars).
  • Target height from estimated earth surface.
  • Speed range and track properties
  • RCS Size.

10 frames, 1 Hz update Rate, 10 Sec. continuous. Each point represents a moving object.
Digital AESA + massive computations

- In previous slides, digital AESA tries to mimic analog AESA. Today’s CPU is 10,000 times better than CPU in 2000.
- Compressive sensing requires $10^5$ times computations compared to beamforming for 1000 RTX.

- Ultra-fine spatial/velocity- resolution in the same aperture.
AESA Radar Future Trends

- Analog AESA
- Hybrid AESA
- All-Digital AESA
- Ultra-Thin All-Digital AESA

Future AESA:
- > $10^4$-times memory + computation
  - Long-range Hypersonic Threats
  - Mid-range Slow Moving Threats
  - Electronics Warfare: EA, ES, EP

Form Factors:
- Thick
- Thin

Complexity:
- Low
- High

Timeline:
- ~1990
- ~2000
- ~2010
- Present
- Working on
Agenda

• Technology Progress Overview.

• Market Segmentation.

• Testing Challenges.
This section will be updated during presentation.
Summary

- Technology progress enables large-aperture phased array in ultra-thin formfactor, and enhancing many existing and new applications.

- Future phased array market will be segmented into three major sectors:
  - Digital full array: computation intensive high performance market.
  - Digital sparse array: computation intensive low cost market
  - Hybrid array: power efficient satellite market.

- Ultrathin array testing will not only rely on Keysight’s high-performance equipment’s (e.g. PNA-X), array products will have extensive built-in-self-test, system-level adaptive algorithm, software-intensive system-level environment testing simulation framework, and innovative production testing mechanics to drive normalized array cost by a factor of four in the next decade.